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EXAMINER	
KEBEDE, BROOK	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/716,843
Filing Date: November 17, 2000
Appellant(s): IKEDA ET AL.

James H. Walters
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed May 26, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 5, 6, 8 and 9 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,786,237	Cockerill et al.	7-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

a. Claims 5, 6, 8, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Cockerill et al. (US/5,786,237).

Re claim 5, Cockerill et al. disclose a method for manufacturing the semiconductor device, comprising: a step forming a plurality of identical semiconductor chips on a semiconductor wafer (see Fig. 1); a step of carrying out a quality test for each of a plurality of said semiconductor chips formed on said semiconductor wafer (see Fig. 6); and a step of dividing one or a plurality pieces of said semiconductor chips on the basis of a result of said quality test, wherein said plurality of semiconductor chips are divided into first groups made of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but wherein said chips are divided into second groups made of two pieces if four pieces are determined to be not possible to form a group as a result of said step of carrying out a quality test but if two pieces are determined to be possible, and wherein said chips are divided into third groups made of one piece if neither four pieces nor two pieces are determined to be possible to form a group as a result of said step of carrying out a quality test but if one piece is determined to be possible as a result of said quality test (see Figs. 1-7; Col. 3, line 21 – Col. 4, line 62).

Re claim 6, as applied to claim 5 above, Cockerill et al. disclose all the claimed limitations including the limitation wherein said semiconductor chips are memory chips (see Figs. 1-7; Col. 3, line 21 – Col. 4, line 62).

Re claim 8, Cockerill et al. disclose a method for manufacturing the semiconductor device, comprising: a step forming a plurality of identical semiconductor chips on a semiconductor wafer (see Fig. 1); a step of carrying out a quality test for each of a plurality of said semiconductor chips formed on said semiconductor wafer; a step of carrying out wiring, resin sealing and terminal formation on the semiconductor chips formed on the semiconductor wafer (see Fig. 6); and a step of dividing one or a plurality pieces of said semiconductor chips on the basis of a result of said quality test, wherein said plurality of semiconductor chips are divided into first groups made of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but wherein said chips are divided into second groups made of two pieces if four pieces are determined to be not possible to form a group as a result of said step of carrying out a quality test but if two pieces are determined to be possible, and wherein said chips are divided into third groups made of one piece if neither four pieces nor two pieces are determined to be possible to form a group as a result of said step of carrying out a quality test but if one piece is determined to be possible, after said quality test is carried out (see Figs. 1-7; Col. 3, line 21 – Col. 4, line 62).

Re claim 9, as applied to claim 8 above, Cockerill et al. disclose all the claimed limitations including the limitation wherein said semiconductor chips are memory chips (see Figs. 1-7; Col. 3, line 21 – Col. 4, line 62).

(11) Response to Argument

Appellants' argument filed on May 26, 2004 with respect to rejections of claims 5, 6, 8, and 9 under 35 U.S.C. § 112 second paragraph is moot because the rejection that was set forth in the Office action that was mailed on June 27, 2003 is withdrawn.

Appellants' arguments filed on May 26, 2004 with respect to rejections of claims 5, 6, 8, and 9 under 35 U.S.C. § 102 have been fully considered but they are not persuasive.

I.

A.

Pertaining to appellants' argument on 7-11, with respect to claims 5, 6, 8, and 9, i.e., "While the Cockerill et al. document does mention dividing into 1x4 or 1x3 or 1x2 or lxl, it does not specifically state that it would make the division as a result of the testing as do applicant's claims, making 4 element divisions if possible, but if not, making 2 element or 1 element divisions. The cited document, in contrast, appears to be pre-set for cutting a specific size pattern, either lx4, 1x3, lx2 or lxl. It does not teach that a decision is made based on testing of whether groups of 4 pieces are possible, and if not, then whether groups of 2 are possible, and if not, then into single pieces. Therefore, applicant's claimed invention is different ..."

In response to the appellants' argument, the examiner respectfully submits that such an argument is not commensurate with the scope of the rejected claims as shown above because Cockerill et al. '237 teach all the claimed limitations of the instant application. The examiner respectfully submits that the instant application claimed invention is fully disclosed by Cockerill et al. '237 as depicted in Figs. 1-7 and the supporting specification.

The independent claims, i.e., claims 5 and 8 recite as the following:

Claim 5. A method for manufacturing the semiconductor device, comprising: a step forming a plurality of identical semiconductor chips on a semiconductor wafer; a step of carrying out a quality test for each of a plurality of said semiconductor chips formed on said semiconductor wafer; and a step of dividing one or a plurality pieces of said semiconductor chips on the basis of a result of said quality test, wherein said plurality of semiconductor chips are divided into first groups made of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but wherein said chips are divided into second groups made of two pieces if four pieces are determined to be not possible to form a group as a result of said step of carrying out a quality test but if two pieces are determined to be possible, and wherein said chips are divided into third groups made of one piece if neither four pieces nor two pieces are determined to be possible to form a group as a result of said step of carrying out a quality test but if one piece is determined to be possible as a result of said quality test.

Claim 8. A method for manufacturing the semiconductor device, comprising: a step forming a plurality of identical semiconductor chips on a semiconductor wafer; a step of carrying out a quality test for each of a plurality of said semiconductor chips formed on said semiconductor wafer; a step of carrying out wiring, resin sealing and terminal formation on the semiconductor chips formed on the semiconductor wafer; and a step of dividing one or a plurality pieces of said semiconductor chips on the basis of a result of said quality test, wherein said plurality of semiconductor chips are divided into first groups made of four pieces if four pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but wherein said chips are divided into second groups made of two pieces if four pieces are determined to be not possible to form a group as a result of said step of carrying out a quality test but if two pieces are determined to be possible, and wherein said chips are divided into third groups made of one piece if neither four pieces nor two pieces are determined to be possible to form a group as a result of said step of carrying out a quality test but if one piece is determined to be possible, after said quality test is carried out.

For practical purpose, the examiner respectfully submits Figs. 1, 6, and 7 from Cockerill et al. '237 disclosure.

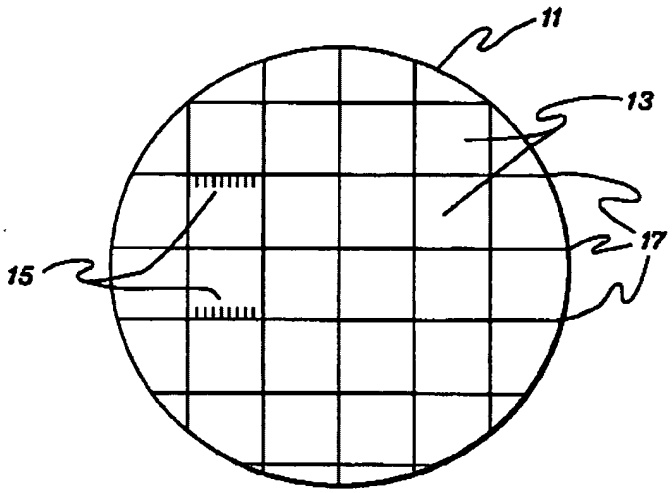

fig. 1

As depicted in Fig 1 above, Cockerill et al. '237 disclose the limitation "a step forming a plurality of identical semiconductor chips on a semiconductor wafer;"

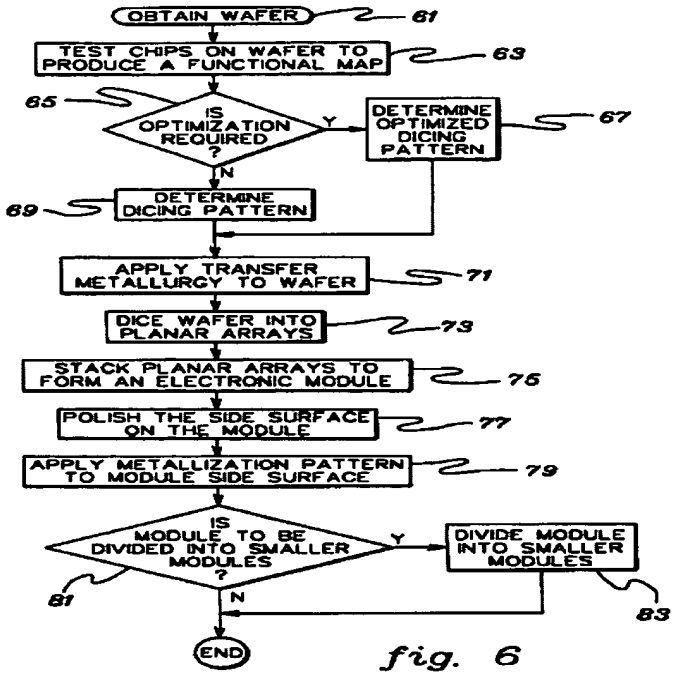

fig. 6

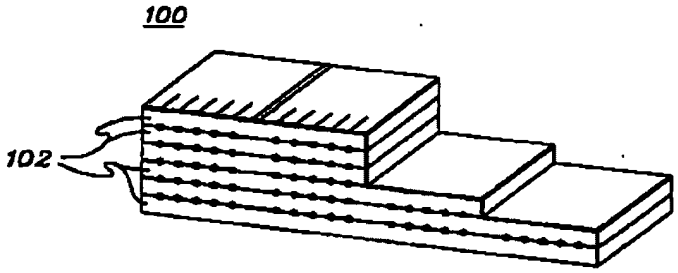

fig. 7

As shown above in Fig. 6, Cockerill et al. '237 disclose the limitation "a step of carrying out a quality test for each of a plurality of said semiconductor chips formed on said semiconductor wafer (see Fig. 1; Fig. 6) (i.e., steps **61** and **63** of Fig. 6 includes drawing of Fig. 1, i.e., a step of carrying out a quality test for each of a plurality of said semiconductor chips formed on said semiconductor wafer); and a step of dividing one or a plurality pieces of said semiconductor chips on the basis of a result of said quality test (see step **65**, **67** and **69**), wherein said plurality of semiconductor chips are divided into first groups made of four pieces if four

pieces are determined to be possible to form a group as a result of said step of carrying out a quality test, but wherein said chips are divided into second groups made of two pieces if four pieces are determined to be not possible to form a group as a result of said step of carrying out a quality test but if two pieces are determined to be possible, and wherein said chips are divided into third groups made of one piece if neither four pieces nor two pieces are determined to be possible to form a group as a result of said step of carrying out a quality test but if one piece is determined to be possible as a result of said quality test" (see Col. 3, line 21 – Col. 6, line 37).

In addition, Cockerill et al. '237 specifically disclose that the reason why and how the decision of dicing pattern of the wafer is conducted after obtaining a test result as depicted in Fig. 6.

In accordance with the present invention, the wafer is first tested to determine which of the plurality of integrated circuit chips are functional. This step is necessary because some chips may exhibit defects, and their inclusion in the resulting electronic module of the present invention may be undesirable. In this regard, a "functional map" indicating functional and non-functional chips within the wafer is produced. This map is then utilized, together with information regarding the dimensions of the planar arrays of IC chips required (see, for example, the 1×4 array of FIG. 2), to produce a "dicing pattern" which indicates how the wafer is to be cut into individual planar arrays of IC chips.

Various manual and/or computer controlled methods may be used to determine a dicing pattern. As a particular process example, if a 1×4 (one chip by four chips) planar array is needed, contiguous linear groups of 4 functional chips are identified. Each group is then designated as part of the dicing pattern. It should be generally noted that each array within the wafer should be oriented in the same direction. That is, no two arrays should be positioned in a perpendicular direction to each other on the wafer. This is necessary to simplify the later process step of applying a transfer metallurgy layer to the wafer.

As an enhancement, an optimizing algorithm (i.e., clustering algorithm) may be used in reorganizing the dicing pattern to optimize the total yield of (e.g., 1×4) arrays from the wafer. For example, the algorithm could automatically calculate the preferred orientation of planar arrays on the wafer.

(see Col. 3, lines 21-50)

As shown above, Cockerill et al. '237 clearly disclose that "In accordance with the present invention, **the wafer is first tested to determine which of the plurality of integrated circuit chips are functional**. **This step is necessary because some chips may exhibit defects, and their inclusion in the resulting electronic module of the present invention may be undesirable**. **In this regard, a "functional map" indicating functional and non-functional chips within the wafer is produced**. **This map is then utilized, together with information regarding the dimensions of the planar arrays of IC chips required** ... **to produce a "dicing pattern" which indicates how the wafer is to be cut into individual planar arrays of IC chips.**"

Contrary to appellants' argument, i.e., "the cited document, in contrast, appears to be pre-set for cutting a specific size pattern," Cockerill et al. '237 clearly disclose the decision of the dicing pattern is due to testing result that particularly to eliminate the defective chip(s) in the wafer. Therefore, the examiner respectfully submits that appellants' argument has no merit in this aspect.

Further, in response to appellants' argument that "Nowhere does Cockerill et al. discuss dividing into groups of 4, 2 or 1 depending on the results of a quality test. Cockerill et al merely divide the wafer to produce as may of a single array size (1x4 is the given example) that is currently desired to be produced. It does not teach or suggest dividing the wafer groups into the largest size (4, 2, or 1) that is possible given the results of testing...," the examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above.

In this particular case, claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

As claimed in claims 5 and 8, "group(s)" in the claim limitation does not have any special meaning. The specification of the instant application, in Page 3 lines 17-25, states the following:

> **It is preferable that semiconductor chips, particularly memory chips, according to the result of quality test are divided in every group made of four pieces if four is possible to handle, every two pieces if four is impossible but two are possible to handle, and every one piece if two are impossible to handle. As described above, priority of dividing in a group of a plurality of pieces makes efficient manufacture of the semiconductor device of the large (for four pieces) unit possible.**

As clearly shown above, the claimed invention of the instant application dices the wafer into four-pieces of chips together or two-pieces of chips together according to the test result. Similarly, Cockerill et al. '237 discloses dicing pattern of the wafer into four-pieces of chips together (1x4), into three-pieces of chips together (1x3), into two-pieces of chips together (1x2), or a sing-piece of chip (1x1) according to the test result. (See Cockerill et al. '237 Figs. 6 and 7; Col. 4, line 51 – Col. 6, line 36). Any of these diced chips can fall into any group of the diced chips pattern. Hence, appellants' argument in this regard has no merit.

In summary, as set forth in the Office action that was mailed on June 27, 2003 and fully argued herein above, Cockerill et al. '237 teach all the claimed limitations of the instant

application. Therefore, the rejection of claims 5, 6, 8, and 9 under 35 U.S.C. 102 is deemed proper.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Technology Center 2800

Appeal conference has been held on July 27, 2004. The conferees listed herein below.

1. Olik Chaudhuri, SPE Art Unit 2823. OC
2. Wael M. Fahmy, SPE Art Unit 2814. W.F
3. Brook Kebede, Examiner Art Unit 2823. BK

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August 9, 2004

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